Filing Date: December 7, 2001
Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Assignee: Intel Corporation

REMARKS

This responds to the Office Action mailed on May 19, 2005.

Claims 12-14 and 18-25 are canceled. Claims 1-11, 15-17 and 26-30 are pending in this application.

§103 Rejection of the Claims

Claims 1, 3-9 and 11 were rejected under 35 USC § 103(a) as being unpatentable over Greene et al. (U.S. 5,670,993) in view of Emerson et al. (U.S. 6,664,969) and Larson et al. (U.S. 5,563,727). Any proposed combination asserted for purposes of rendering claims obvious must be operational as proposed by the Examiner and must not run contrary to the teachings of the references comprised within the proposed combination.

First, Applicants would like to reiterate and point out again that the Emerson reference specifically teaches a synchronous approach to updating an image. If an asynchronous approach were used in Emerson then the asserted benefits of the teachings of Emerson would be lost because Emerson could not integrate with legacy VGA architectures. The very purpose of Emerson is its ability to integrate with legacy architectures. Therefore, Applicants believe the proposed inclusion of Emerson with Larson is improper and cannot be achieved in the manner cited by the Examiner because to do so would defeat the very teachings and purpose of Emerson. Moreover, since the Examiner is relying on a combination that includes both the Emerson and the Larson references for purposes of rendering Applicants' independent claims 1 and 9 obvious, the rejection cannot be sustained because the combination cannot be properly achieved.

Second, the Greene reference relies on flag bits for each bit of an image and scans each flag when performing a complete refresh operation. The entire teaching and technique in Greene relies on these flags and their processing. If Greene is modified to include a sparse refresh using asynchronous updates, then the teachings and techniques presented in Greene are lost. In other words, one of ordinary skill in the art would not have read Greene in view of Larson to achieve Applicants' invention because to do so would have required an entire reworking of the techniques presented in Greene and would have resulted in an entirely new approach where the flags on each bit were not needed and/or not processed in the manners taught in Greene. That is,

Dkt: 884.607US1 (INTEL)

Serial Number: 10/010,524

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

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Applicants respectfully believe that the proposed modifications sought by the Examiner for purposes of achieving the asserted combination of references could have only been achieved via improper hindsight after one of ordinary skill in the art read and comprehended Applicants' invention. Hindsight is improper and therefore cannot be used to render Applicants' invention obvious. Therefore, Applicants do not believe that a proposed combination of Greene and Larson is permissible, and Applicants respectfully request that the rejections of independent claims 1 and 9 be reconsidered and the claims allowed.

Third, Larson is directed to an Active Matrix Liquid Crystal Display (AMLCD). The technique presented in Larson is directed to a specific type of display and the improvement of image quality therein utilizing minimum power consumption. The context of the location cited within Larson by the Examiner for purposes of teaching asynchronous updates to images is made while describing converting an image from alternating current to direct current. Larson, col. 11, lines 50-52. Applicants do not believe that one of ordinary skill in the art would have read this portion of Larson outside the context of this conversion process within which it is being described within Larson.

Moreover, the asserted asynchronous update is achieved in Larson via a specific circuit architecture that is presented in FIG. 10B of Larson. That is, Larson relies on specific circuit architecture to achieve its asserted asynchronous update without that circuit architecture there is no other teaching of asynchronous updates within Larson. So, if Larson is combined with Greene and Emerson the only way asynchronous updates can be achieved is with the Larson circuit architecture and within the context of converting from alternating current to direct current. Moreover, and as was previously noted, Emerson relies on only synchronous updates and Greene relies on specific flags for each bit of an image to determine updates in a synchronous fashion.

Therefore, Applicants do not believe that the proposed combination of Larson, Greene, and Emerson can be achieved without running contrary to the individual teachings of the references and without substantial and undue reworking of the references in view of improper hindsight after having read and comprehended Applicants' invention. Furthermore, any achieved combination would necessarily have to include the circuit architecture of Larson used for purposes of converting from alternating current to direct current and such architecture is not the positively recited claim limitations cited in Applicants' independent claims 1 and 9.

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Accordingly, Applicants respectfully request that the rejections with respect to independent claims 1 and 9 be withdrawn and the claims be allowed.

Claims 2, 10, 15-17 and 26-30 were also rejected under 35 USC § 103(a) as being unpatentable over Greene et al., Emerson et al. and Larson et al. in view of Perego (U.S. 5,835,082). Again, a proposed combination of references is not properly made if the combination runs contrary to the teachings of the individual references and if it cannot be achieved in the manner proposed by the Examiner.

First, Applicants note that claim 2 is dependent from independent claim 1 and that claim 10 is dependent from independent claim 9; therefore, for the remarks presented above with respect to independent claims 1 and 9, the rejections of claims 2 and 10 should be withdrawn.

Applicants would like to incorporate by reference previous arguments made by the Applicants above and in previous responses with respect to the Greene, Emerson, and Perego references.

The rejection of Applicants' independent claims 15 and 26 rely on combining Greene, Emerson, and Larson. Applicants have detailed above why Applicants do not believe that such a combination is permissible and why even if such a combination were made the resulting combination would not include the limitations of Applicants' independent claims. In summary, Emerson relies on synchronous updates for its teachings, Greene relies on flags for each bit of an image that are each scanned and processed during a refresh, and Larson can only achieve an asynchronous update with specific circuit architecture. Accordingly, the proposed combination of Emerson, Greene, and Larson is not proper and even if made still must be made within the context of converting from alternating current to direct current and with circuit architecture presented and taught in Larson. Therefore, the rejections of Applicants' independent claims 15 and 26 should be withdrawn and the claims allowed.

Page 9
Dkt: 884.607US1 (INTEL)

AMENDMENT AND RESPONSE UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE

Serial Number: 10/010,524

Filing Date: December 7, 2001

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Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney, Joseph Mehrle at (513) 942-0224, or Applicants' below-named representative to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

THOMAS E. WILLIS ET AL.

By their Representatives,

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Date July 19 2005

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450,

Alexandria, VA 22313-1450, on this 19th day of July 2005.

Name

Signature